What is claimed is:

1. A method comprising:

initializing a circuit said circuit having at least one memory element coupled to a memory bus on a host system;

monitoring signals on the memory bus;

detecting a first sequence of signals; and

switching control of the at least one memory element to the circuit.

2. The method of claim 1 further comprising:

detecting a second sequence of signals; and

switching control of the at least one memory element to the host system

3. The method of claim 2 wherein error correcting codes are switched off prior to switching control of the at least one memory element to the host system.

4. The method of claim 1 wherein initializing a circuit having at least one memory element coupled to a memory bus on a host system comprises detecting a sequence of writes to memory locations on the circuit.

5. The method of claim 4 wherein the sequence of writes are writes to random memory locations on the circuit.

6. The method of claim 1 wherein monitoring signals on the memory bus comprises the circuit monitoring control, address, and data signals on the host system.

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7. The method of claim 1 wherein detecting a first sequence of signals comprises detecting at least one write signal to a particular memory location on the circuit.

8. The method of claim 1 wherein detecting a first sequence of signals comprises detecting at least one read signal from a particular memory location on the circuit.

9. The method of claim 1 wherein switching control of the memory bus to the circuit comprises a processing element in the circuit reading from or writing to the memory in the circuit.

10. The method of claim 2 wherein switching control of the at least one memory element to the host system comprises a processor on the host system reading from or writing to the at least one memory element.

11. An apparatus comprising:

a memory bus on a host system;

a plurality of memory elements on a circuit, said plurality of memory elements communicatively coupled with the memory bus;

a processing element on the circuit communicatively coupled with the plurality of memory element and the memory bus, said processing element to

monitor signals on the memory bus;

detect a first sequence of signals; and

switch control of the plurality of memory elements to the circuit.

12. The apparatus of claim 11 further comprising said processing element to detect a second sequence of signals; and
switch control of the plurality of memory elements to the host system.

13. The apparatus of claim 12 wherein error correcting codes are switched off prior to switching control of the plurality of memory element to the host system.

14. The apparatus of claim 11 wherein the processing element is at least one of a field programmable gate array, and a processor.

15. The apparatus of claim 11 wherein the processing element to monitor signals on the memory bus comprises the processing element to monitor control, address, and data signals on the host system.

16. The apparatus of claim 11 wherein the processing element to detect a first sequence of signals comprises the processing element to detect at least one write signal to a particular memory element on the circuit.

17. The apparatus of claim 11 wherein the processing element to detect a first sequence of signals comprises the processing element to detect at least one read signal to a particular memory element on the circuit.

18. The apparatus of claim 11 wherein the processing element to switch control of the plurality of memory element to the circuit comprises the processing element reading from or writing to the plurality of memory elements.

19. The apparatus of claim 12 wherein the processing element to switch control of the plurality of memory elements to the circuit comprises a processor on the host system reading from or writing to the plurality of memory elements.

20. An article of manufacture comprising:

a machine-accessible medium including instructions that, when executed by a machine, causes the machine to perform operations comprising

initializing a circuit said circuit having at least one memory element coupled to a memory bus on a host system;

monitoring signals on the memory bus;

detecting a first sequence of signals; and

switching control of the at least one memory element to the circuit.

21. The article of manufacture as in claim 20, further comprising instructions for detecting a second sequence of signals; and

switching control of the at least one memory element to the host system.

22. The article of manufacture as in claim 21, further comprising instructions for switching of error correcting codes prior to switching control of the at least one memory element to the host system.

23. The article of manufacture as in claim 20, wherein said instructions for initializing a circuit having at least one memory element coupled to a memory bus on a host system comprises further instructions for detecting a sequence of writes to memory locations on the circuit.

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24. The article of manufacture as in claim 23, wherein said instructions for detecting a sequence of writes include further instructions for writing to random memory locations on a circuit.

25. The article of manufacture as in claim 20, wherein said instructions for monitoring signals on the memory bus comprises further instructions for the circuit monitoring control, address, and data signals on the host system.

26. The article of manufacture as in claim 20, wherein said instructions for detecting a first sequence of signals comprises further instructions for detecting at least one write signal to a particular memory location on the circuit.

27. The article of manufacture as in claim 20, wherein said instructions for detecting a first sequence of signals comprises further instructions for detecting at least one read signal from a particular memory location on the circuit.

28. The article of manufacture as in claim 20, wherein said instructions for switching control of the memory bus to the circuit comprises further instructions for a processing element in the circuit reading from or writing to the memory in the circuit.

29. The article of manufacture as in claim 21, wherein said instructions for switching control of the at least one memory element to the host system comprises further instructions for a processor on the host system reading from or writing to the at least one memory element.